CLAIMS

1. Self aligned MIS transistor (1) having a source zone (16,30,34) and a drain zone (18,32,36) on either side of a channel zone (20), as well as a T shaped gate structure comprising a vertical bar (6) located above the channel zone (20), surmounted by a horizontal bar (8) extending on either side of the vertical bar (6), said horizontal bar (8) having a lower part (81), a lateral part (82) and an upper part (83), the gate structure consisting of a stacking of one or several conductive layers (69), a base zone of the gate structure being defined as being around the base of the vertical bar (6) of the T, transistor in which the gate structure is coated with a shaping material (14), said material covering the vertical bar (6) of the T, and the lower (81) and lateral (82) parts of the horizontal bar (8) of the T,

characterised in that said shaping material (14) also covers the base zone of the T shaped structure.

2. Self aligned MIS transistor (1) according to claim 1, characterised in that the base zone covered by the shaping material (14) extends above the source (16,30,34) and drain (18,32,36) zones.

3. Self aligned MIS transistor (1) according to claim 1, characterised in that the first extension zones (42, 44) between the channel (20) and source and drain (16, 18) zones respectively have a doping of the same nature as the source and drain zones (16, 18) but weaker.

4. Self aligned MIS transistor (1) according to claim 1, characterised in that the second extension zones (45, 46) between the channel (20) and source and drain (16, 18) zones

respectively have a doping of nature opposite to that of the source and drain zones.

5. Self aligned MIS transistor (1) according to claim 3, characterised in that the second extension zones (45, 46) between the first extension zones (42, 44) and the channel zone (20) have respectively a doping of nature opposite to that of the source and drain zones(16, 18).

6. Self aligned MIS transistor (1) according to claim 1, characterised in that the shaping material is of silicon nitride (Si_3N_4) or hafnium oxide (HfO_2) or zirconium oxide (ZrO_2) or aluminium oxide (Al_2O_3).

7. Self aligned MIS transistor (1) according to claim 1, characterised in that the stacking of layers constituting the gate structure lodged in the shaping material (14) is intrinsic poly silicon or a metal.

8. Method for manufacturing, on a semiconductor substrate (2), at least one self aligned MIS transistor (1) having a source zone (16,30,34) and a drain zone (18,32,36) on either side of a channel zone (20), as well as a T shaped gate structure of low resistivity comprising a vertical bar (6) located above the channel zone (20), surmounted by a horizontal bar (8) extending on either side of the vertical bar (6), said horizontal bar (8) having a lower part (81), a lateral part (82) and an upper part (83), the gate structure consisting of a stacking of one or several conductive layers (69), a base zone of the gate structure being defined as being around the base of the vertical bar (6) of the T, the method comprising a step of forming a solid shape having the T shape of the grid that one wishes to form, and the coating of said shape in a shaping material (14), said shaping material (14) coating the lateral surface (62) of the vertical bar (6) of

the T, the lower (81) and lateral (82) surfaces of the horizontal bar of the T,

characterised in that said shaping material (14) also covers the base zone of the definitive gate structure.

9. Method according to claim 8 characterised in that the shaping material covers a part at least of the source and drain zones(16, 18).

10. Method according to claim 8 characterised in that the shaping material is silicon nitride (Si_3N_4) or hafnium oxide (HfO_2) or zirconium oxide (ZrO_2) or aluminium oxide (Al_2O_3).